REMARKS/ARGUMENTS

The Applicants gratefully acknowledge the Examiner's allowance of claims 19-23 and the Examiner's indication of allowable subject matter in claims 8-10 and 18. Reconsideration of the rejected claims is hereby requested.

Recitation of the Invention as-claimed:

One aspect of the invention, as recited in claim 1, is an imager system that is provided in a semiconductor substrate. The imager system includes a plurality of photosensitive, charge-integrating pixels that are arranged in rows and columns of a pixel array for capturing illumination of a scene to be imaged. Each pixel includes a photogenerated charge accumulation region of the substrate and a sense node at which an electrical signal, indicative of pixel charge accumulation, can be measured without discharging the accumulation region.

There is provided pixel access control circuitry that is connected to the pixel array rows and columns to deliver pixel access signals generated by the access control circuitry for independently accessing a selected pixel in the array.

An input interface circuit is connected to accept a dynamic range specification input for the pixels. Integration control circuitry is configured to generate, based on the input dynamic range specification from the input interface circuit, pixel-specific integration control signals delivered to a selected pixel, independent of other pixels. The integration control circuitry is connected to access a selected pixel of the array to read the sense node electrical signal of the selected pixel.

An output interface circuit is connected to the pixel array to produce output image data that is based on sense node electrical signals from the pixel array.

Rejections of the Claims:

Claims 1-7 and 11-17 were rejected under 35 U.S.C. §103(a) as being unpatentable over Lee et al., U.S. Publication 2002/0101528 (hereinafter "Lee") in view of Umeda et al., U.S. Patent No. 6,452,632 (hereinafter "Umeda") and Katsuma, U.S. Patent No. 5,398,123 (hereinafter "Katsuma").

The Examiner suggested that Lee describes an imager system provided in a semiconductor substrate and having a plurality of photosensitive charge integrating pixels in a pixel array. Each pixel in the Lee array was said by the Examiner to include a photogenerated charge accumulation region and a sense node at which an electrical signal indicative of pixel charge accumulation can be measured without discharging the accumulation region. Lee was said to describe pixel access control circuitry, provided as a pixel addressing module 16 and a timing and control module 50, connected to pixel array rows and columns to deliver pixel access signals for independently accessing a selected pixel in the array.

The Applicants concur with this characterization of Lee with the exception of the characterization that Lee can independently access selected pixels. In Lee's explicit description of the sensor operation, at P. 2, ¶33, Lee explains that the sensor is operated by applying a transfer signal to all the pixels in a row to move the charge from each pixel photodiode in that row to a sensing node for each of the pixels. A reset signal is then applied to all of the pixels in the row by the row bus. Lee emphasizes this operation at P. 2, ¶28, where it is stated that the image is read out by having a row select signal provide the address for a selected row on the row bus to set a row to the active state. This is the conventional operation of an image sensor, with all pixels in a row being reset. In other words all pixels residing in a common row are accessed together. Independent accessing of a selected pixel as required by the claims is not taught or suggested by Lee.

At Lee P. 2, ¶30 referred to by the Examiner, Lee suggests that the image sensor can be programmed for an x-y windowed set of pixels. This does not imply that a selected pixel can be independently accessed. The row-by-row control of Lee's pixel array does not allow for independent pixel control and thus row-by-row control would be employed even for an x-y windowed pixel array.

The Examiner suggested that Lee describes integration control circuitry, provided as an interface ASIC 82 and a micro-controller 81, that are connected to access a selected pixel of the array to read the sense node electrical signal of the selected pixel. The Applicants respectfully submit that the Examiner likely has misidentified the functionality of Lee's ASIC and micro-controller. The micro-controller 81 and ASIC 82 referred to by the Examiner are taught by Lee to be employed for "digital processing of digital data that is output from the camera on-a-chip system," (Lee P. 3, ¶37). It is the timing and control module 50 and the pixel addressing module 16 just described that control and access pixels, not the ASIC or micro-controller. The Examiner appears to agree with this characterization in his description of the timing and control module 50 and the pixel addressing module 16 as "pixel access control circuitry." Lee explains that the timing and control module is programmed by the micro-controller with commands that traverse the Serial Interface and Control module (P. 3, ¶39, col. 2).

As explained above, in Lee's imager operation, a transfer signal is applied to all the pixels in a selected row to move the charge from each pixel photodiode in that row to a sensing node for each of the pixels. This enables reading the sensing node of pixels in a selected row. In other words, the sense node electrical signal of a selected pixel is read in conjunction with the sense node electrical signals of the other pixels in the selected pixel's row. The Applicants concur that Lee teaches access and reading of the sense node electrical signal of a selected

pixel, but that such is accomplished along with reading of the sense node electrical signals of the other pixels in a common row.

The Examiner asserts that Lee's ASIC and micro-controller are configured to generate pixel-specific integration control signals to be delivered to a selected pixel, independent of other pixels as required by the claims. Lee does not teach or even suggest the generation of pixel-specific integration control signals, let alone integration control signals that would be delivered to a selected pixel independent of other pixels. First, as just explained, Lee controls pixel integration by resetting pixels on a row-by-row basis: at P. 2, ¶ 33 referenced above, Lee explains that a common row bus is employed for controlling a row of pixels, and that the row bus enables application of a reset signal to the pixels in the row once the charge from the sensing nodes of the pixels in the row are sent to a source follower amplifier input. This resetting of pixels in a row is the integration control employed by Lee. Each Lee pixel in a row is reset simultaneously. Lee does not send an integration control signal, here a reset signal, to a selected pixel independent of other pixels. Lee sends a reset signal to every pixel in a selected row simultaneously.

Further, Lee does not provide integration control circuitry configured to generate pixel-specific integration control signals. As just explained, a common reset signal is sent to every pixel in a common row. Lee explains that the sensing node output of each pixel in a row to a source follower amplifier as is typical within the art of Active Pixel Sensors (P. 2, ¶ 33). Lee does not teach or suggest anything but employing a pixel array-wide common reset signal as is conventional - all pixels in the entire array are controlled by a reset signal that is the same for every pixel. Lee does not teach or suggest otherwise. But the claims require a configuration for generating an integration control signal that is specific to a selected pixel and that is delivered only to the selected pixel, independent of other pixels in a common row or elsewhere in the pixel array.

The Examiner appeared to rely on the fact that Lee's imager is a CMOS APS imager to imply that Lee teaches a configuration for independently controlling and accessing specific pixels independent of other pixels, here with row and column address circuits. The Examiner referred to Lee Col. 4, lines 16-19 and 25-31. These passages do not appear to be directly relevant and the Applicants believe this may have been a typographical error in the Examiner's Action. As just explained, Lee explicitly states that his APS imager is operated in a conventional manner. Conventionally, and as explained by Lee, each pixel in a row is reset simultaneously, with a common array-wide integration reset.

The Examiner suggested that Lee provides a configuration for generation of pixel-specific integration control signals by setting exposure conditions. Lee explains at P. 2, ¶32 that the timing and control logic module controls resetting of pixels relative to the frame rate, controls the mode of pixel integration for each frame, and controls a photometer mode for adjustment of electronic shuttering. All of these controls - pixel reset for a selected frame rate, a selected mode of pixel array integration, and array electronic shuttering - are necessarily set for the entire pixel array. The entire Lee array is controlled to meet frame rate, or a selected integration mode, or electronic shuttering. Lee also explains that a photometer mode can be employed for setting exposure conditions - a pixel-array-wide condition (P. 2, ¶29). Nowhere does Lee even hint at a configuration for generation of pixel-specific integration control signals as required by the claims. Lee only generates integration control signals that are common to his entire pixel array or that portion of the array in operation.

The Examiner also rebutted the Applicants earlier assertion and attested that Lee teaches that the micro-controller 81 and ASIC 82 can be formed as part of the camera on-a-chip system, i.e., formed on a common semiconductor substrate. The Applicants now recognize this attribute of Lee and concur with the Examiner.

The Examiner suggested that Lee's integration control signals are based on input signals that are provided by a Human and Camera Control Interface. Lee does not once describe or even mention the Human and Camera Control Interface - it is completely missing from Lee's description. One can only make assumptions based on the diagram of Lee Fig. 3. In that diagram, it is shown that the Human and Camera Control Interface is configured for communication with the micro-controller 81. Even if for the sake of argument it is assumed that the operation of the timing and control logic module described at Lee P. 2, ¶32 is set by the Human and Camera Control Interface, to control resetting of pixels relative to the frame rate, control the mode of pixel integration for each frame, and control a photometer mode for adjustment of electronic shuttering, all of these controls - are set by Lee for the entire pixel array. Nowhere does Lee describe a configuration for generation of pixel-specific integration control signals or delivery of such control signals to a selected pixel independent of other pixels as required by the claims.

The Examiner affirmed that Lee's Human and Camera Control Interface is not formed as part of a camera-on-a-chip system, i.e., is not integrated in a semiconductor substrate as required by the claims. The Examiner further affirmed that Lee does not show an input interface circuit connected to accept a dynamic range specification input for array pixels as required by the claims.

The Examiner ignored a further requirement of the claims: the claims require integration control circuitry that is configured to generate pixel-specific integration control signals based on a dynamic range specification input provided by the input interface circuitry. It is not enough to input a dynamic range or to generate pixel-specific integration control signals. The claims require that the integration control signals be generated based on a dynamic range specification. Lee completely fails on all of these counts.

The Examiner suggested that Umeda teaches the integration of sensor, signal processing, and input interface modules into a single chip. The Applicants concur that Umeda teaches sensor, signal processing, and input interface modules integrated into a single chip.

The Examiner suggested that Katsuma teaches an imager system including an input interface circuit section for accepting a dynamic range specification input for a CCD scanner. This is not correct.

Katsuma teaches a system and technique for acquiring, or "reading," an image with a CCD scanner, processing the acquired, scanned, image to reproduce the scanned image color favorably, and outputting the processed image to a color laser printer (Col. 3, lines 38-41). Katsuma's system includes a keyboard and parameter setting I/O port 6 from which various commands and instructions can be inputted by an operator (Col. 3, lines 50-53).

The operation of Katsuma's system is diagrammed in the flow chart of Katsuma Fig. 3 and in the description at Col. 5, lines 22-38 as referenced by the Examiner. In brief, an image is first scanned into a CCD scanner, and then based on the dynamic range of the CCD scanner, the acquired image is digitally processed to adjust the color levels of the scanned image. Once the color levels are adjusted, the image is then printed out at a color laser printer. Katsuma does not teach or suggest the generation of integration control signals based on an input of dynamic range as required by the claims. Katsuma teaches the adjustment of color levels of a scanned image based on dynamic range.

Katsuma explains that the dynamic range options for his scanner-printer system are displayed on a CRT and an operator inputs a selected one of the ranges: "The inputted dynamic range determines the range of the original image density to be used in processing the original image," (Col. 5, lines 29-32). An "image density signal" is the "dot percent" for each color of a printed image (Col.

1, lines 27-30). In other words, the dynamic range input by an operator determines the dot percent density of each color for which a scanned image is to be processed for printing by the color laser printer.

The dynamic range input by an operator does not provide for generation of integration control signals as required by the claims. Instead, the original image data scanned by the CCD that is within the selected dynamic range is expressed in 8 bit data with 1-255 tonal levels for digital image processing (Col. 5, lines 32-34). The CCD image acquisition is not controlled by the dynamic range input; the CCD operates to scan an image independent of the dynamic range input. Then the digital image data that has been acquired by the CCD is output to the image processor selectively, with only that image data falling within the input dynamic range being digitized and stored in the image memory of the image processor as red (R), green (G) and blue (B) components of the scanned image (Col. 5, lines 42-45).

It is unambiguously clear that Katsuma employs an input dynamic range for digital image processing and not for generation of integration control signals as required by the claims. Katsuma explains that at step S7, a scanned image undergoes "masking processing" to adjust color levels. The "masking coefficients α" take on different values depending on the dynamic range that was input to the system (Col. 4, lines 35-37). Katsuma's masking coefficients are said to change with the dynamic range that is set for an input device (Col. 8, lines 61-62). As explained above, the input dynamic range sets the 1-255 tonal levels of color that are stored from a scanned image, and thus that set the masking coefficients for digitally adjusting the color levels. The dynamic range does not control generation of integration control signals for the CCD imager as required by the claims.

The Examiner suggested that it would be obvious to employ an interface circuit to accept a dynamic range specification like that of Katsuma with the

array pixels of Lee. The Applicants respectfully submit that there is clearly no motivation for combining the dynamic range input of Katsuma with the camera-on-a-chip system of Lee. Katsuma employs a dynamic range input for enabling digital post-processing of an acquired image to enhance the color levels of the image prior to its printing by a color laser printer. Katsuma's dynamic range input sets the digitized color levels of an image scanned by a CCD scanner that are accepted by a digital image processor - no control of the image acquisition by the CCD scanner is enabled by the dynamic range input.

Lee does not teach or even hint at digital post processing of an acquired image to adjust color levels of the image; Lee is concerned solely with integration of components of a conventional CMOS APS imager on a chip. There is no teaching or even suggestion of a reason to combine the teachings of Katsuma and Lee. The Examiner suggested that Lee's imager would have "more advantages" by obtaining an image with visually favorable quality as Katsuma teaches. But the Examiner failed to recognize that to produce a visually favorable quality in the manner of Katsuma, a digital image processing unit is required; Lee does not provide such. The dynamic range specification employed by Katsuma for image storage in an image processing unit would be meaningless if applied to Lee.

But even if the teachings of Katsuma, Umeda, and Lee are combined for the sake of argument, the combination fails to teach or even suggest the requirements of the claims. As explained previously, the Examiner is required to consider the invention as a whole, and further cannot ignore particular elements of the claims, *MPEP 2141.02*. The question under 35 U.S.C. §103 is not whether differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. *Stratoflex, Inc., v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983). When the invention is properly considered as a whole, including all of the recited limitations of claim 1, there is provided an imager system having a pixel array, pixel access control circuitry, an

input interface circuit, integration control circuitry, and an output interface circuit that are all provided in a semiconductor substrate.

The Examiner has ignored the claim requirement that the integration control circuitry be configured to accept a dynamic range specification input and generate pixel-specific integration control signals based on the dynamic range specification input, and that the pixel-specific integration control signals must be delivered to the selected pixel independent of other pixels. In the imager system of the invention, the integration control circuitry is connected such that when a user inputs a dynamic range specification, the integration control circuitry generates a corresponding pixel integration control signal and delivers the signal to the selected pixel independent of other pixels. This aspect of the integration control circuitry recited in claim 1 was ignored by the Examiner. The Examiner is not permitted to ignore limitations of the claims, and must consider the invention as a whole *MPEP 2141.02.*

None of Lee, Umeda, or Katsuma, considered separately, teach or even suggest integration control circuitry configured to accept a dynamic range specification input and generate pixel-specific integration control signals based on the dynamic range specification input, with the pixel-specific integration control signals delivered to the selected pixel independent of other pixels as required by the claims. No combination of Lee, Umeda, or Katsuma overcomes this failure, and thus the claims are clearly distinguished over a combination of Lee, Umeda, and Katsuma.

With regard to claim 2, the Applicants concur that Umeda's pixels enable production of a voltage signal; but this does not provide the missing features required by claim 1, from which claim 2 depends. With regard to claim 3, the Applicants concur that Lee's pixels and Umeda's pixels can be CMOS pixels; but this does not provide the missing features required by claim 1, from which claim 3 depends. With regard to claim 4, the Applicants concur that the pixel-specific

integration control signals of Lee are reset signals; but this does not provide the missing features required by claim 1, from which claim 4 depends.

With regard to claim 5, the Examiner suggested that Lee's imager system includes an array of memory cells, with each memory cell corresponding to a specified pixel in a pixel array and connected to store from the integration controller an indication of the number of reset occurrences of the specified pixel during a given integration period as required by the claim. This is not the case. The Examiner points to Lee's buffer memory 85 shown in Lee Fig. 3, and refers to Lee P. 3, ¶37. Lee there explains that a buffer memory 85 may be included to throttle the data from the Analog to Digital Converter ADC 86. In other words, the digitized image data is sent through the buffer memory for output to "Digital Data Out" and, if necessary, stored at the buffer memory to await an output command. Lee describes this previously, at P. 3, ¶35, indicating that the temporary digital storage can be used to buffer the pixel value data.

Lee does not teach or even hint at storing an indication of the number of reset occurrences of a specified pixel during a given integration period as required by claim 5. Lee's buffer memory 85 stores the pixel value itself, not the number of times a pixel has been reset.

All of claims 6-10 depend from claim 5. It has been demonstrated just above that Lee fails to provide the array of memory cells required by claim 5, and therefore Lee fails to meet that requirement also made by claims 6-10.

In the invention as required by claim 6, a memory cell array that is spatially separate from the pixel array is provided storing an indication of the number of reset occurrences, as shown in Fig. 1 of the instant application. But as just explained, Lee does not at all store a number of reset occurrences; Lee simply stores pixel values themselves.

Claim 7 requires that the output interface circuit includes an image data formatter that is configured to generate output image data based on pixel sense node signals and reset occurrence data from the memory cell array. Lee does not employ a memory cell array for tracking reset occurrence data, and thus fails the requirements of claim 7 for generating output image data based on data from a memory cell array. As explained above, the data formatter of Lee simply stores digitized pixel values and can format such for output; but no formatting based on reset occurrence data is taught or suggested by Lee.

Claims 11-13 all depend from claim 1 and therefore include all of the limitations of claim 1. Claim 11 further requires that the output interface circuit include a correlated double-sampling circuit that is configured to convert pixel sense node signals from single-ended to differential output and to remove any pixel reset level from the sense node signals. Claim 12 requires that the output interface circuit further include an analog-to-digital converter that is configured to digitize pixel sense node signals. Claim 13 requires that an array of analog-to-digital converters be provided with a multiplexer connected to this array for directing pixel sense node signals to a selected converter in the array of converters.

The Applicants concur that Lee describes the use of a correlated double-sampling circuit and the use of an analog-to-digital converter or array of converters in connection with the output of pixel sense node signals. But Lee does not fill in the features missing from the Lee-Umeda-Katsuma combination discussed above and required by claims 11-13 as-dependent from claim 1.

Claims 14-17 all depend from claim 1 and therefore require all of the limitations of claim 1. Claim 14 further requires that the input interface circuit be connected to accept a specification of a sub-array of pixels to be controlled in the pixel array. Here the integration control circuitry is connected to independently access a selected pixel in the sub-array of pixels. Claim 15

requires that the input interface circuit be connected to accept a specification of a number of pixels to be controlled in the pixel array. Here the integration control circuitry is connected to independently access a selected pixel in the number of pixels specified. Claim 16 requires that the input interface circuit be connected to accept a specification of a frame rate at which images are to be produced. Here the integration control circuitry is connected to impose an imager integration period based on the frame rate specification. Claim 17 requires that the input interface circuit be connected to accept a specification of sense node electrical signal digitization resolution with the output interface circuit here including an image data formatter that is configured to generate digitized output image data based on sense node electrical signals and the digitization resolution specification.

The Examiner suggested with regard to claims 14-17 that Lee, Umeda, and Katsuma disclose all subject matter as discussed "with respect to same comment as with claim 1." Each of claims 14-17 makes specific requirements of the input interface circuit of claim 1, as recited above. But Lee, Umeda, and Katsuma, considered alone or in any combination, fail to teach an input interface circuit connected to accept a dynamic range specification input for array pixels for generating pixel-specific integration control signals based on the input dynamic range specification and delivered to a selected pixel, independent of other pixels as required by claim 1. For any of the input interface connections required by claims 14-17, this connection required by claim 1, from which claims 14-17 depend, fails to be taught or suggested by the references.

The Applicants therefore submit that none of Lee, Umeda, or Katsuma, taken alone or in any combination, teach or suggest the invention as recited in the claims. The Applicants therefore submit that the claims are in condition for allowance, which action is requested.

If the Examiner has any questions or would like to discuss the claims, he is encouraged to telephone the undersigned Agent directly at his convenience at the phone number given below.

Respectfully submitted,

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